2019 Paper E2.1: Digital Electronics II

Answer ALL questions.

There are THREE questions on the paper.

Question ONE counts for 50% of the marks, other questions 25% each

Time allowed: 2 hours

(Not to be removed from the Examination Room)

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.
4. Signed binary numbers use 2's complement notation.

1. (a) An 8-bit microprocessor system with an 18-bit memory address bus A[17:0] is interfaced to two banks of RAM (RAM1 and RAM2), one bank of ROM, and a space for input and output (IO) as shown in *Figure 1.1a*. The control signals from the microprocessor are omitted for clarity.

The address decoder module generates four enable signals for the RAM, ROM and IO: EN_RAM1, EN_RAM2, EN_ROM and EN_IO, implementing the following Boolean equations:

EN_RAM1 = ~A17 & ~A16 & ~A15

EN_RAM2 = ~A17 & ~A16 & A15 &~A14

EN_ROM = ~A17 & A16

EN_IO = A17 & A16 & A15 & A14 & A13 & A12 & A11 & A10 & A9 & A8 & A7 & A6 &A5

(i) Using the interface shown in *Figure 1.1b*, design the address decoder in Verilog HDL.

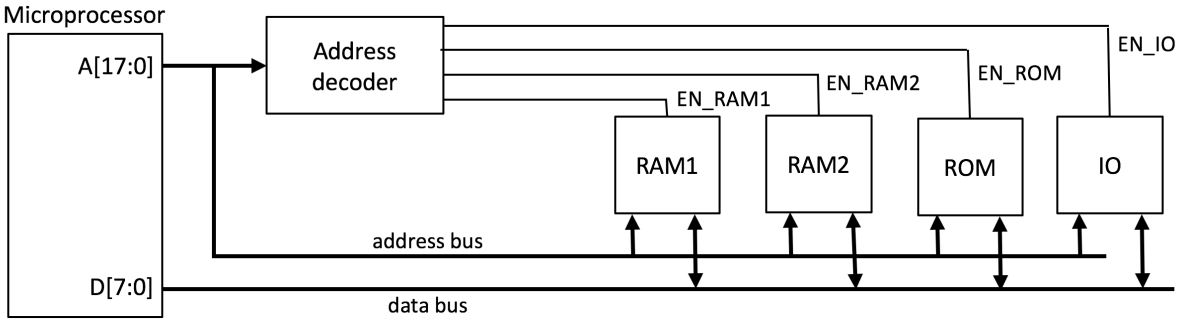
[2]

(ii) Determine the address ranges selected by the four enable signals.

[4]

(iii) The two blocks of RAM are to be implemented using only 16k x 8 RAM chips. Draw the circuit diagram for RAM1 and RAM2 showing how the address bus, the data bus, and the enable signals EN_RAM1 and EN_RAM2 are connected to the RAM chips.

[4]



(a)

```
module decoder (a, en_ram1, en_ram2, en_rom, en_io);

   input [17:0]  a;
   output en_ram1, en_ram2, en_rom, en_io;
```

(b)

Figure 1.1

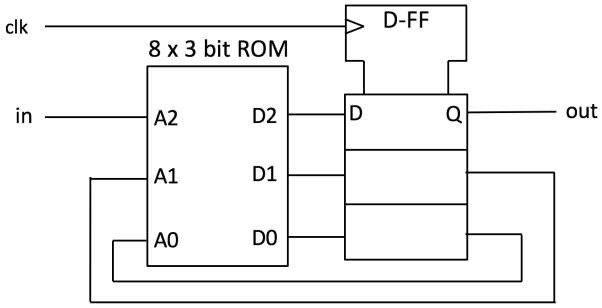
(b) *Figure 1.2* shows the circuit that implements a finite state machine (FSM) which has four states, one input ***in***, and one output ***out***. The circuit consists of an 8 x 3-bit ROM and three D-flipflops clocked by a common clock signal ***clk***. The contents of the ROM are shown in the table in *Figure 1.2*. The four states are encoded in binary code as S0, S1, S2 and S3. The D-FFs are initially cleared on power up.

(i) Derive the state diagram for the FSM.

[5]

(ii) Starting with the state diagram in (i), design a new version of the FSM in Verilog HDL.

[5]



Address A[2:0]	Data D[2:0]
000	000
001	000
010	000
011	101
100	101
101	010
110	111
111	000

Figure 1.2

(c) *Figure 1.3* shows the Verilog HDL implementation of a 5-bit pseudo-random binary sequence (PRBS) generator circuit.

(i) Draw the circuit schematic diagram for the PRBS generator.

[4]

(ii) Determine the output value Q5:1 for the first 6 clock cycles.

[4]

(iii) What is the primitive polynomial of this PRBS generator?

[2]

```
module prbs (clk, Q);

   input          clk;
   output [5:1]   Q;

   reg [5:1]      sreg;

   initial sreg = 5'b1;

   always @ (posedge clk)
      sreg <= {sreg[4:1], sreg[2] ^ sreg[5]};

   assign Q = sreg;
endmodule
```

Figure 1.3

(d) *Figure 1.4* shows a circuit with two D-flipflops FF1 and FF2 with setup and hold times of 3 ns and 2 ns respectively, and a clock-to-Q output delay of 1 ns. The clock signal CLK has a 1:1 mark-space ratio. The D input of FF2 is driven by logic_A, which has a propagation delay between 1 ns and 4 ns. The clock input to FF2 is driven by logic_B, which has a propagation delay between 2 ns and 8 ns.

(i) Derive the setup time constraint for D input of FF2 as an inequality.

[4]

(ii) By considering the setup time constraint only, derive the maximum operating frequency f_{max} of CLK.

[2]

(iii) Derive the hold time constraint for the D input of FF2, and show why there can be a hold time violation if the maximum operating frequency derived in (ii) is used.

[4]

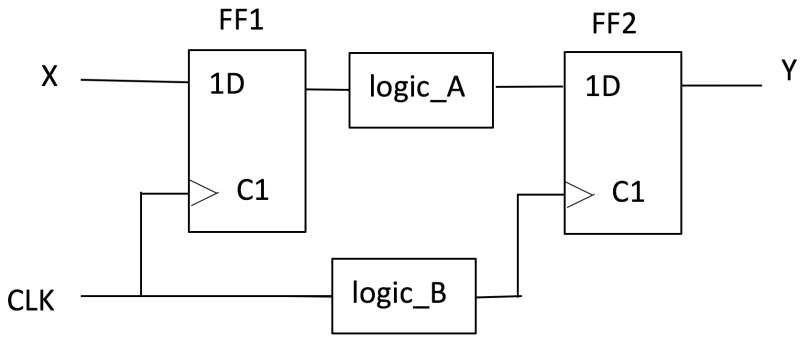


Figure 1.4

(e) (i) Explain the principle of operation of a 12-bit pulse-width modulation (PWM) digital-to-analogue converter (DAC).

[5]

(ii) Design in Verilog HDL a PWM DAC using the interface shown in *Figure 1.5*.

[5]

```
module pwm_dac (clk, data_in, pwm_out);

   input          clk;       // system clock
   input [11:0]   data_in;   // input data for conversion
   output         pwm_out;   // PWM output
```

Figure 1.5

2. *Figure 2.1a* shows the block diagram of a circuit that produces a pair of sinusoidal signals exactly π/2 radians apart (they are known as quadrature signals). The circuit consists of a dual-port 1024 x 9-bit ROM, a 10-bit binary counter, a binary adder and a clock divider circuit as shown. The clock divider divides the 50MHz system clock by a factor of K. The binary adder adds a constant value N to the counter output cnt[9:0]. The ROM stores the coefficient values for one complete cycle of a sinewave in 2's complement form and has a Verilog HDL interface shown in *Figure 2.1b*.

a) Explain how this circuit works.

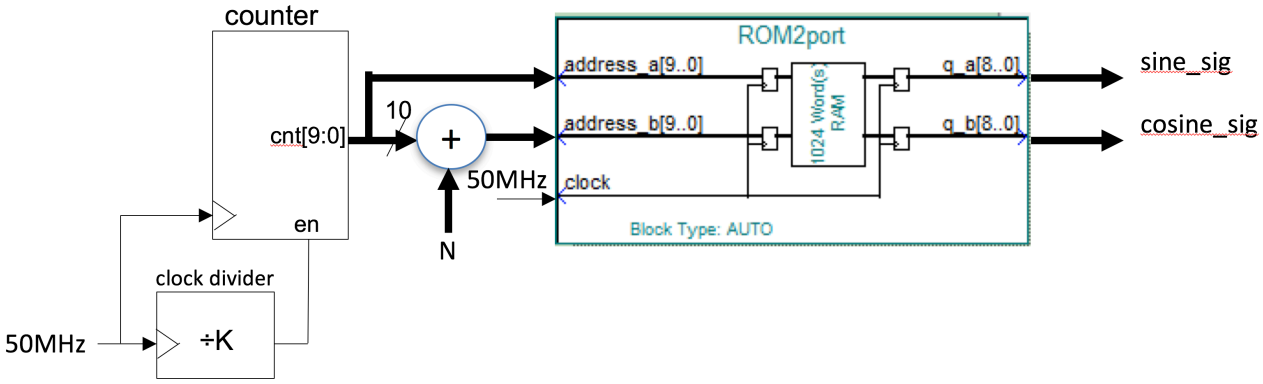
[10]

b) If you are required to produce the sine and cosine signals at a frequency closest to 10kHz, determine the value of N and K.

[5]

c) Implement in Verilog HDL, the circuit shown in *Figure 2.1a*. State to 4 significant digits the frequency of the output signals.

[10]



(a)

```
module ROM2port (
    address_a,
    address_b,
    clock,
    q_a,
    q_b);

    input [9:0]  address_a;
    input [9:0]  address_b;
    input   clock;
    output   [8:0]  q_a;
    output   [8:0]  q_b;
```

(b)

Figure 2.1

3. *Figure 3.1* shows a channel in a vending machine through which coins are rolled down and detected by three light sensitive detectors. The timing diagram for the signals X, Y, Z from the three detectors Dx, Dy and Dz when 10p, 20p and 50p coins are respectively fed into the machine in that order are given in *Figure 3.2*. The detectors are so positioned that only waveforms X, Y, Z as shown are possible. A synchronous finite state machine (FSM) is used to generate the three output signals p10, p20 and p50 as shown in *Figure 3.2* to indicate the type of coin being detected.

   You may assume that a clock signal of suitably high frequency is available. In addition, the detectors are arranged in such a way that the rising edge of Z is at least one clock cycle before Y, and the rising edge of Y is at least one clock cycle before X. When a coin is detected, one of the three outputs goes high shortly after the falling edge of Z for one clock period. Also, assume that these are the only three types of coins ever used, and that only one coin can roll down the channel at any one time.

   (a) Design the FSM to produce the signals p10, p20 and p50 in the form of a state diagram using 7 states. State any assumptions used.

   [15]

   (b) Using one-hot encoding, implement your design in Verilog HDL.

   [10]

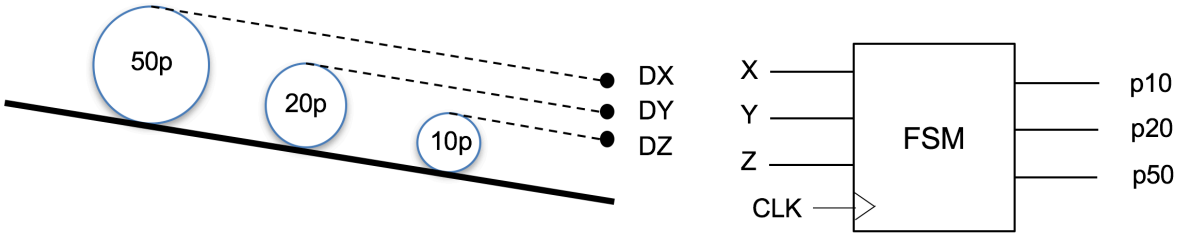


Figure 3.1

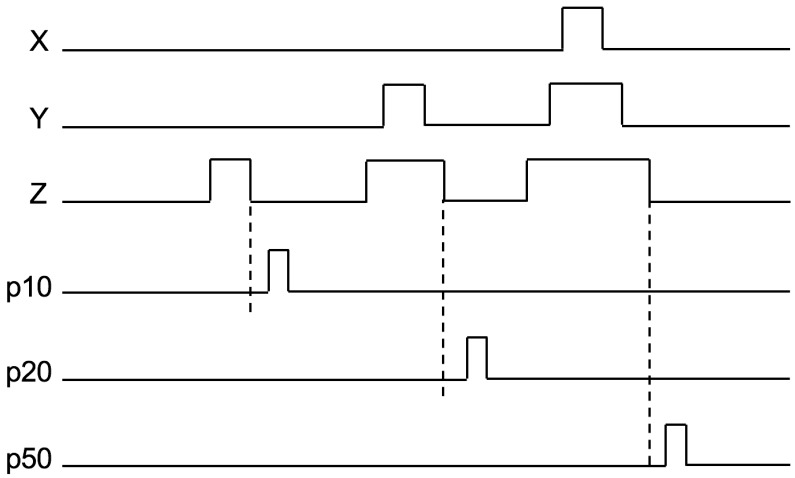


Figure 3.2